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FOREIGN TECHNOLOGY DIVISION

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by

Thanasis Kamburelis and Andrzej Zasada

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Thanasis Kamburelis, Andrzej Zasada
(MERA-ELWRO) Wroclaw

The article presents the ODRA 1300 (ODRA 1304, 1325, and 1305) and JS 1032 computer systems currently produced by the MERA ELWRO works in Wroclaw. The most important problems connected with the logic architecture, design, technology and programming of the above-mentioned systems are specified in this article.

A Little Bit of History on the MERA-ELWRO Enterprise's 15th Anniversary

The first computers produced by the MERA-ELWRO enterprise came into being in 1963, These were the UMC-1 machines or so-called machines of the 1st generation whose design was based on the electronic tube.

Since then a lot has been changed not only in the logic design, programming, design and technology, but also in the computer production and its operation.

In the above-mentioned period the MERA-ELWRO enterprise switched from the 1st generation computers through the 2nd generation ones (e.g. ODRA 1204, 1304) to the 3rd generation ODRA 1305 and 1325, (whose design is based on the integrated systems of the integration standard scale) and in the current year this enterprise has begun a serial production of the Uniform System modernized computer which is designated by number JS-1032 (or briefly R-32) where the integrated systems with the medium integration scale have been used.

The computer structure has changed from the serial logical structures to the parallel ones, from the single-program computers to the multiple-programmed ones, from the single-computer systems to the multiple-computer system and multiple-access ones.

In the stage of preparation there are the systems with the multiple-level memory organization and with the memory dynamic division. Due to these innovations these systems will become very effective in operation and maintenance.

The operational speed of the computers produced by the MERA-ELWRO enterprise for the above-mentioned period has increased as much as about 6,000 times and the cost of a million additions has decreased from 500 zlotys up to .0028 zlotys which is equal to 170,000 times. The structure of the cost of the computer medium configuration has changed as well. The first digital machines consisted mainly from the central unit whose cost was equal to 94 per cent of the whole set cost and from simple outside installations (mostly teletypes or a device for the paper tape). However, the sets of the outside installations have grown to the extent when their cost is equal to 70 per cent of the cost of the entire configuration of the computer besides an enormous increase of the equipment of the central unit itself.

THE ODRA 1300 COMPUTER SYSTEMS.

The ODRA 1300 computer system which consists of the ODRA 1304,1325 and 1305 central units as well as of a number of outside installations is nowadays a basic equipment for the realization of the country's information program. To the end of the current year the MERA-ELWRO enterprise will produce about 330 computer sets belonging to the ODRA 1300 system. This system's popularity is continuously growing among the consumers. Despite that this system's initial concepts of the logic design were developed more than 10 years ago, this popularity owes not only to good technical solutions but also (and maybe first of all) to the fact that the above-mentioned system has a wide and verified basic programming as well as the programming which can be applied in the most

various fields of administration and planning, of the automatization of the project works, of the scientific-technical computations, of the control over the technological processes, etc.

The equipment and program sources of the ODRA 1300 system designed by the MERA-ELWRO enterprise or by other enterprises, institutions or center of the higher education enable to create different configurations applicable both to the traditional transformation that is the local one (Fig.1) and to the remote transformation (Fig.2) in a flexible and economical way.

THE EMC UNIFORM SYSTEM.

The Electronic Digital Machines Uniform System(JS EMC) consisting of a number of central units with the differentiated computing power, BUT WITH an identical logic design, and WITH common operational principles as well as consisting of a set of outside installations is the fruit of scientific, technological and industrial collaboration of socialist countries.

The first Polish machine of the Uniform System is the R-32 digital machine. The R-32 machine similarly to the R-20, R-30, R-40 and R-50 machines in respect of the function belong to the so-called first generation of the Uniform System machines (RIAD-I). The above-mentioned computers fully possess the uniform logic design, though they base themselves on different solutions of the design as well as on different technologies of the generation. Due to the uniform logic design it has become possible to accept a uniform programming on the machine instruction level as well. However, the R-10 and R-20A machines are not comformable from the point of view of the program with the rest of computers.

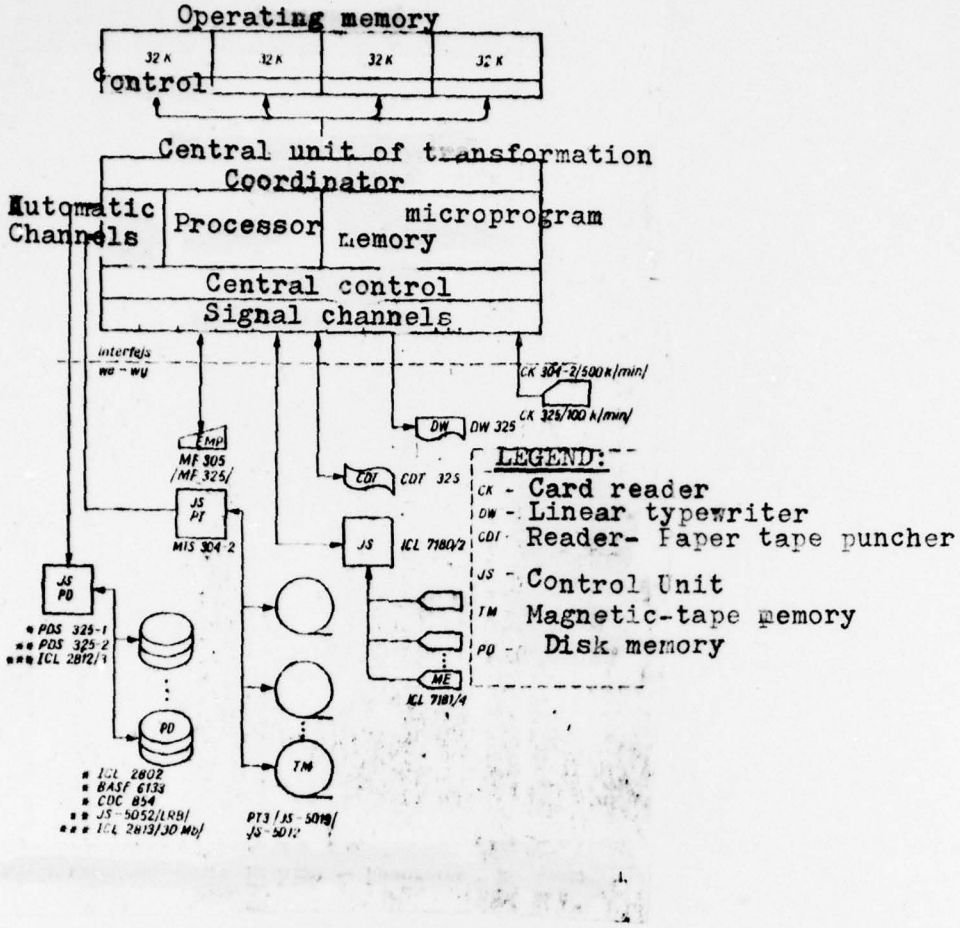

Fig.1. The ODRA 1305(1325) computer. The conventional configuration.

The R-10 computer is not conformable for the reason of the application of different illegal instructions(preferential).

The acceptance of the conformable logic design for the majority of the central units and this of the outside devices as well as the uniform programming has created practical possibilities to concentrate the scientific and technical personnel and industrial potential of the socialist countries (Bulgaria, Czechoslovakia, GDR, Poland, Hungary and U.S.S.R. and from the beginning of 1974 Cuba and Rumania as well) on the realization of the common and ambitious program which was called "Program RIAD", or the program of Electronic Computing Technology and whose principal task has been to satisfy the collaborating countries in the field of information

The R-32 Uniform System computer of Polish production came into being a little bit later than the rest of the types of the RIAD I system (for the first time it was exhibited during the 1974 International Poznan Fair). Due to this retardation the R-32 computer design could be based on the most modern constructive and technological solutions existing in the country as well as on the integrated elements of the integration medium scale designated as the TTL type. The accepted technological and economic base has helped to achieve high technical and economic factors (e,g. the ratio of speed to the manufacture cost). Due to a high computing capacity the R-32 computer can be included in the medium or large class of the central units depending on the operating memory capacity as well as on the amount of the channels for the information dispatching. The computer speed mounts to about 500,000 additions per second, whereas the average speed according to the Gibson I mixture mounts to more than 200,000 operations per second and the operating memory capacity may fluctuate within the 128Kb up to 1024 Kb limits (See Fig. 3,4 and5).

Inside of the R-32 the following functional means are built in as the standard ones:

the means carrying out the standard commands(that is the operations of the fixed-point arithmetics, the logic operations, displacements, the control operations, the in-and -out operations, etc); the commands of the decimal arithmetics as well as the floating-point arithmetics;

16 universal registers (accumulators) and 4 floating-point registers;

a channel of the byte multiplexor;

three selecting channels;

the operating memory protective means;

the direct control means (for the purpose of relaying or receiving the data directly by the outside installation or the second processor).

the interval timer and other means.

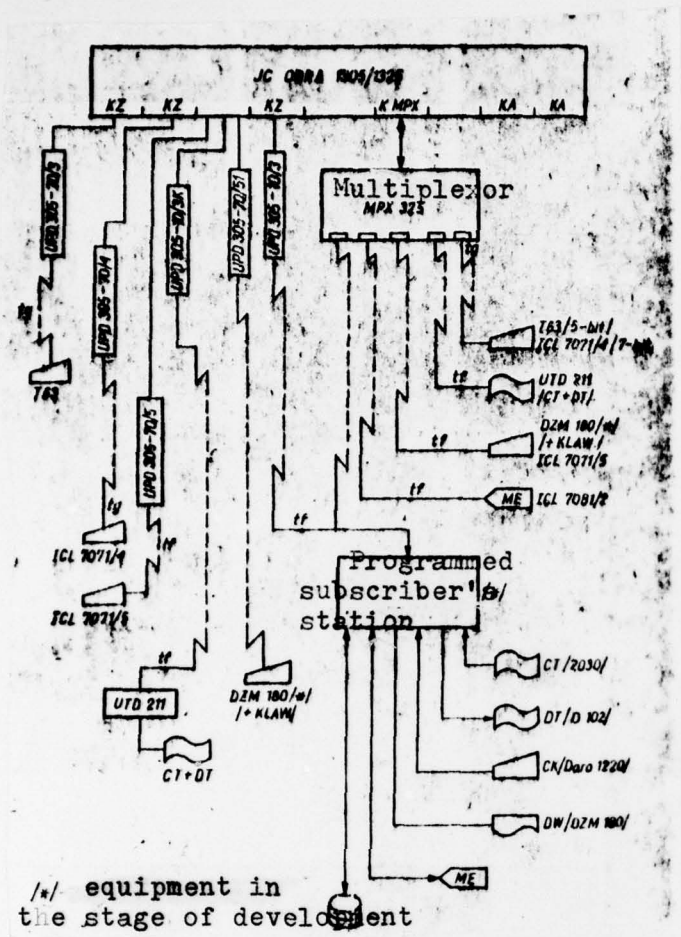

Fig.2 The ODRA 1305(1325) computer. The configuration of teletransformation (in the stage of development)

During the R-32 computer development the application of the element base or the design and technological solutions going ahead of the country's industrial possibilities at 2 or 3 years has been accepted as a general principle. Thanks to the above-mentioned this computer will be technologically modern at the momemt of the initiation of the serial production. At present one can confirm that this principle has been faultless, since almost all sets which are in use in the R-32 computer design even now are included in the serial production in Poland or other socialist countries.

In the computer design the following solutions were accepted:

the integrated elements of the medium(and standard) integration scale;

multiple-layer (up to 12 layers) plates of big size packages

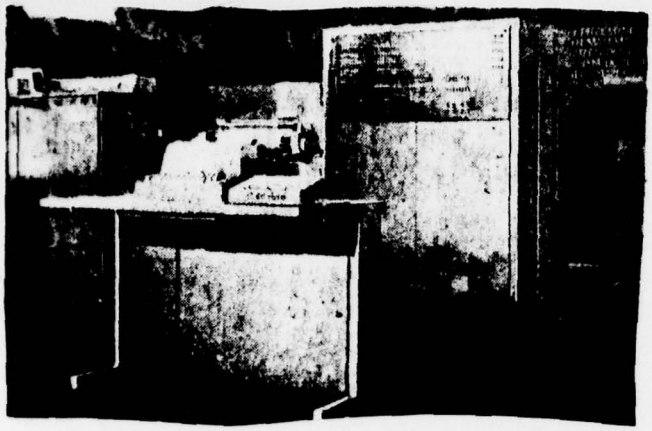

Photo 1. The central unit of the R-32 computer alon with the EC-7070 console

multiple-layer silver plates;

the microprograms fast memory with a big capacity;
capacious operating ferrite-memory of a modern design (so-called planar design);
flat cables to connect computer blocks;
no-cabinet aluminum mechanical design.

The implementation of the above-mentioned principles results in the following characteristics for the R-32 machine;

the machine's high total efficiency;
easiness of widening of the operating memory capacity (to 1024 Kb);
very high efficiency coefficient- the cost (e.g. the processor and channels occupy only 29 logic packages whose dimensions are 295 by 150 mm);
a high reliability;
small size of the central unit (like the middle class machine);
the energy consumption is very small (when the memory capacity is 256 Kb the energy consumption is 3.6 KVA).

The machine local memory (Fig.3) or the working memory is designed on the integrated systems and consists of 64 thirty-two byte words. This memory includes the following: 16 general registers; 4 floating-point registers and 40 working registers for the processor and channels.

The microprogram memory (PAM) is a permanent memory of a transformer type and its cycle is equal to 300 ns. It comprises 2816 eighty-six byte words where both the processor and channel control is coded. The application of the microprogram memory of such a capacity enabled to simplify and diminish the machine logic as well as to provide this machine with certain new (comparatively to other JS EMC machines) characteristics, such as:

periodic check-ups of the machine correct functioning (turns on automatically);
automatic memorization when the machine is in the state of the operating memory (PAO) at the moment of the energy interruption and restoration of this state when the machine is turned on;
special built-in technical tests for the processor and memory.

The microrogram memory (the permanent one) is designed in the transformer technology and located on the 4-layer plates whose size is identical to logic packages.

The permanent memory wholeness consists of 16 packages of the same construction. The difference between them is only in the information cintent which is "sown" in ferrite cores. Every package contains 352 fourty-three byte words. The R-32 machine's permanent memory is characterized by speed action (as for the transformer technology); the access time amounts to 120 ns and cycle time amounts to 300 ns. Due to the application of economical control systems that is when a selection system control 4 words small sizes and low cost of the entire memory have been obtained.

The operating memory (PAO) consists of the logical blocks whose capacity is 128 Kb. Every block with 128 Kb of the operating memory has the designed on integrated systems memory of the protection key (PAK) whose capacity is 64 bytes. Thus in the system the PAK capacity changes proportionally to the PAO capacity. A cycle of the PAO operation (1200 nsek) corresponds to 4 cycles of the processor (4x300 nsek) or the performance of 4 microcommands.

The processor and channels microprograms are designed in such a way that the processor in most cases turns on the contact with PAO, precisely every 4 microcommands. Due to such synchronization the process is deferred by PAO only to a very insignificant degree and PAO seldom 3-byte address is put on the switches and through this method it is possible to fix its address location in the area of the operating memory. In case of the damage of any block it is possible to reoutline the system very fast through changing the the working blocks' addresses and switching the failing ones off.

The operating memory design is based on small ferrite-cores (the diameter .54mm) in so-called planar technology. It consists of locating big amounts of cores on the printed plates and assembling electronic systems in the vicinity from the core-matrix. Among the advantages typical for this system one can name the following:
big capacity of the memory with maintaining small dimensions;
insignificant level of disturbances;
high action speed and significant decrease of the labor-consumption during the operation in comparison with the so-called traditional memories based on the so-called ferrite-block.

Every construction module of the operating memory consists of the plate with the ferrite-matrix and the control plate and this module's capacity amounts to 16 Kbytes (8Kx18 bytes). The PAO logical block with the capacity amounting to 128 Kbytes includes 8 modules, 1 control package, 3 adapter packages. The PAO construction modules at their ends have couplers that provide with the possibility to exchange them which significantly speeds up the detection of damages and their repair.

Processor employs mechanisms and 4-byte tracks. It works in either of 2 operational modes: the CJP mode and the We-WY (in-out) mode. In the CJP mode processor fulfills mocroprogram commands, whereas in the WE-WY(in-out) mode only microprograms of the channel service are fulfilled.

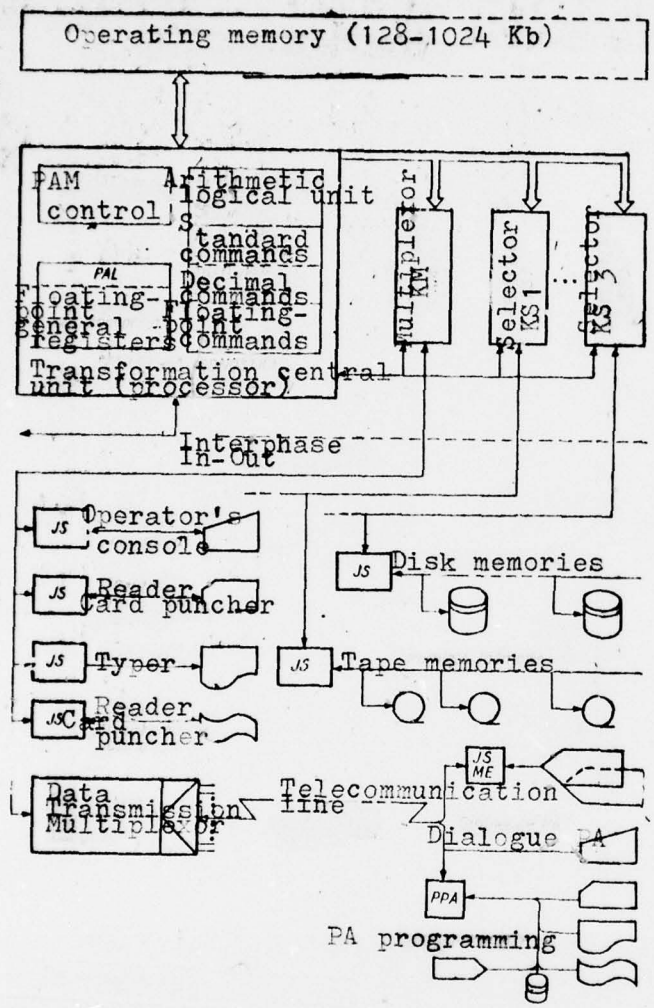

Fig.3. General structure of the JS-1032(R-32) computer

Passage from the WE-WY (In-Out) mode is taking place in a compulsory way, that is on channels' demand and can happen in the process of fulfillment of any command. In this case the current command's microprogram becomes suspended and the following microcommand's address is being rewritten to a special buffer register and the processor begins to fulfill one of the microprograms of the channel service. After the IN-OUT operation is completed the processor resumes the command's suspended microprogram. In the In-Out mode the specified parts of the microcommand are being decoded differently than in the CJP mode. By this it is possible to get an additional collection of microoperations designated exceptionally for the control over channels' operation.

The central control found its solution in such a way that the processor's operation cycle and this of channels was limited only by the sum of the propagation of the information signals and the control itself doesn't cause any additional delays. This is the result of an extra buffer register for the microcommands taken out of the permanent memory. In this way the processor and channels operating with cycle 300 ns use the maximum speed of the permanent memory's operation.

Input-output channels collaborate on one hand with the processor systems and the microprogram memory, on the other hand they control the operation of the outside devices. If a standard version of the R-32 is employed, then 1 multiplexor channel and 3 selector channels are assembled.

The multiplexor channel' operational speed amounts to 110 and 250 Kbytes per second for the multiplexor mode (where many devices are served simultaneously) and for the selector mode(where only one device is served) respectively.

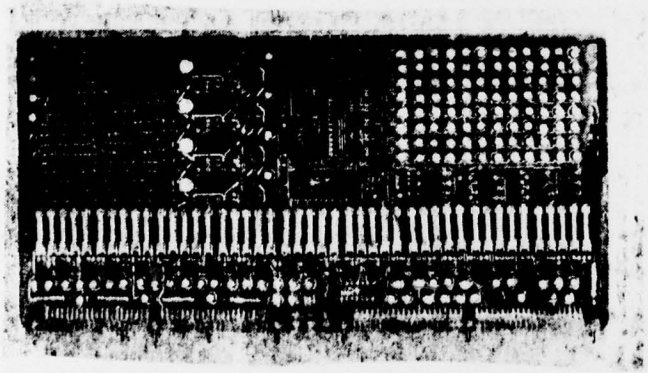

Photo 2. The module package of the microprogram memory (along with transformers,diode matrix,transistor matrix)

As a working memory for the control words of the multiplexor channel the PAO (operating memory) area equal to 2 or 4 Kbytes is in use which is not accessible byusing programs. This enables to store the control words of 128 or 256 subchannels, respectively. The above-mentioned area is always located at the end of the installed operating memory. Such a solution of the multiplexor's memory is very simple and cheap comparatively to the solutions based on the independent memory block.

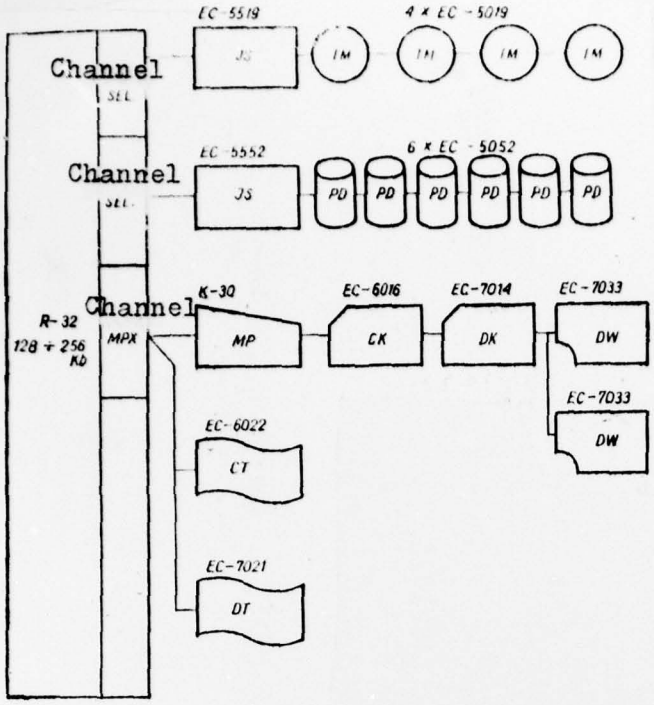

Fig.4. The R-32 computer's typical configuration

Legend:

MP - typewriter
DK - card puncher
CT - tape reader
DT - tape puncher
SEL - selectors
MPX - multiplexer

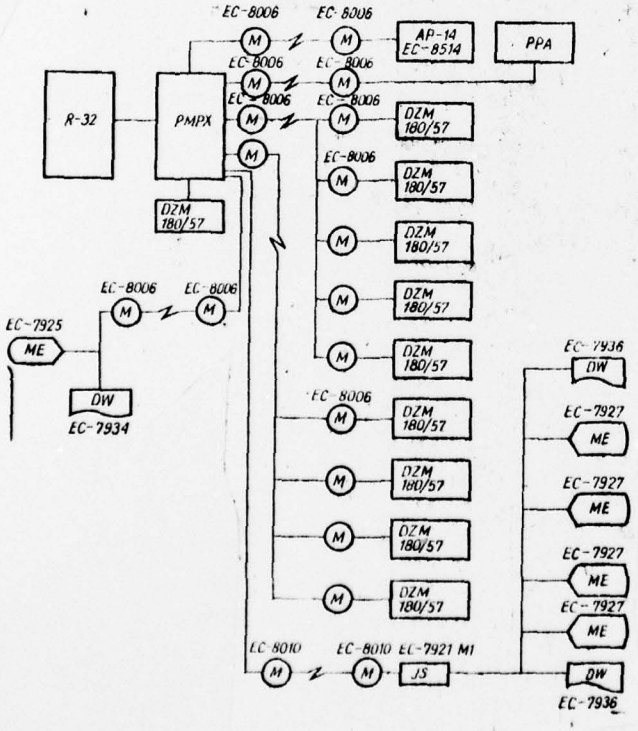

Fig.5 . The R-32 computer's configuration of teletransformation (in the stage of preparation)

Legend:

PMPX - telecommunication multiplexer
AP-14 - Subscriber's station
PPA - Programmed subscriber's station
M - modern
ME - screen monitors

The multiplexor operations are carried out by means of the corresponding microprograms which are stored at the same permanent memory where the processor's microprograms are.

The selector channels have built-in systemic registers controlling the INPUT-OUTPUT operations and they also use the microprograms which are included in the permanent memory. Wide employment of the microprogram control in channels decreases their systemic logic maintaining simultaneously high capacity. The selector channel's dispatch speed amounts 1100 Kbyte/s. However, the total capacity of all channels amounts to 2.6 Mbyte/s., while the theoretical maximum capacity under completely systemic solution could amount 3.3 Mbyte/s.It could increase the channels' cost unproportionally comparatively with the results obtained.

Model		Processor's speed in oper/s.	Operating memory's capacity (in Kb)	Amount and speed of channels (Kb)	
name	code			Multiplexor	Selector
R-10	JS-1010	10000	8 ÷ 64	30	1/200
R-20	JS-1020	9000	64 ÷ 256	16	2/200
R-20A	JS-1021	40000	64 ÷ 256	85	2/250
R-30	JS-1030	55000	128 ÷ 512	40	3/800
R-32	JS-1032	200000	128 ÷ 1024	110	3/1100
R-40	JS-1040	320000	256 ÷ 1024	110	6/1800
R-50	JS-1050	500000	256 ÷ 1024	110	6/1800

Table 1. The JS EMC central units and their main parameters

Footnote 1. The EMC speeds from the R-20 to R-50 are mutually comparable (the Gibson I method), since they use identical size of information as well as a similar list of the maintenance instructions. However the R-10 has a different and simple command list(typical for minicomputers).

Footnote 2. The multiplexor channel's speed is given for the operation in the simultaneous service of many outside devices mode.

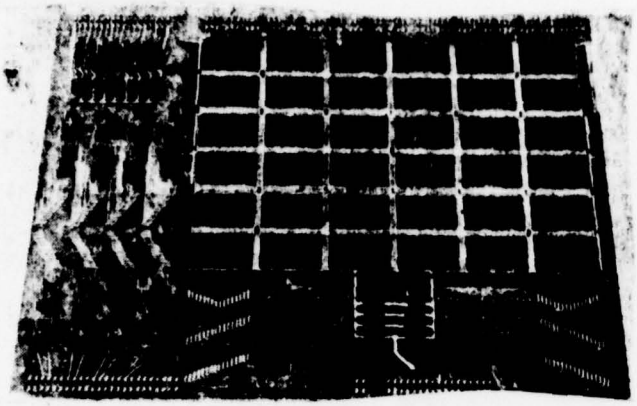

Photo 3. The operating memory's module (16 Kb).

THE CHECK-UP AND DIAGNOSTIC SYSTEM

In order to increase the machine's reliability, besides the traditional oddness check-up a special dynamic check-up as well as the memorization of the machine's state (erratography) that is the state at the moment of an error appearance have been employed. During studies over the R-32's solutions two principle requirements were taken into consideration: the average useful working time cannot be lower than 95 per cent; the average time of the resumption of the machine operation cannot be longer than 30 minutes. In order to meet these requirements different check-up systems as well as diagnostic systems have been built in.

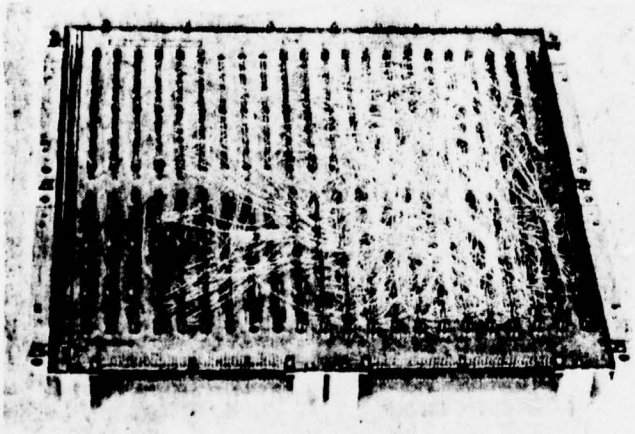

Photo 4. The rear part of the processor plate.

The accepted check-up system embraces very many points of the information flow which enables a permanent verification of the correct machine operation. An error's detection can bring about the machine state erratography, mostly that of the program and activation of the diagnostic

part of the operating system. If a damage is of a temporary nature then the fact of this error's appearance and the ~~performance~~ realization of erratography when this error shows up can be used for statistics of the machine damages. However, in the case of a permanent damage the realization of a number of the program diagnostic procedures enables to localize the damaged element.

Besides continuous check-ups, so-called periodic machine check-up permitting to inspect the arithmometer thoroughly by means of the microprogram tests with a certain frequency (every 20 ms) have also been introduced. The occurence and duration of this test are chosen in such a way that they cannot exceed 1 per cent of the machine functioning time.

In the processor the following elements responsible for the information flow are checked up on the continuous basis:
the systems of the operating memory-processor interphase along with the operating memory;
the information read out from the microprogram memory (PAM);
the systems of the channel microprograms' selection;
the systems of interphase Channel-Units controlling the input-output equipment.

The operating memory possesses the built-in systems making possible an autonomous check-up of the memory physical block by means of a special tester. The check-up follows the logical and physical disconnection of the block from the Operating memory-Processor track. The remaining blocks can function in the system after the completion of reconfiguration by means of the proper switches. Besides this, in the operating memory the processor has a group of tests checking up all blocks of the operating memory by an optional information which is being sent from the keyboard desk or so-called the difficult memory pattern. The signaling existing on the technical desl enables to obtain an error precise localization.

Further more, in the processor there are special built-in signaling registers where errors showing up in different systems are registered. In order to make machines' solutions more "diagnostic", the illegal ~~instruction~~ COMMAND by the name of "DIAGNOZUJ" ("DIAGNOSE!") has been introduced. This command causes the start of the specified diagnostic equipment procedure (e.g. the memorization of the processor registers' state. the channel's state. the local memory's state, the subchannel memory's state, etc).

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